

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				M-11467-2D US		Unassigned	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)			
(Use several sheets if necessary)				Leung et al.			
				Filing Date		Group	
				Filed Herewith		Unassigned	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
RB	AA	4,794,565	12/27/1988	Wu et al.			
	AB	5,029,130	7/2/1991	Yeh			
	AC	5,045,488	9/3/1991	Yeh			
	AD	5,067,108	11/19/1991	Jenq			
	AE	5,120,671	6/9/1992	Tang, et al.			
	AF	5,202,850	4/13/1993	Jenq			
	AG	5,212,541	5/18/1993	Bergemont			
	AH	5,217,920	6/8/1993	Mattox, et al.			
	AI	5,242,848	9/7/1993	Yeh			
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	AL	5,376,571	Dec-94	Bryant et al.			
	AM	5,631,179	May-97	Sung et al.			
	AN	5,741,719	Apr-98	Kim, Keon-soo			
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RB	AZ	6,013,551	1/11/2000	Chen et al.			
Examiner	Richard A. R.		Date Considered 06/25/04				
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>							

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U.S. Patent Documents							
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RB	BA	6,043,536	3/28/2000	Numata et al.	T	T	
	BB	6,054,355	4/25/2000	Inumiya et al.			
	BC	6,057,572	5/2/2000	Ito et al.			
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RB	BQ	S. Aritome, S. Satoh, T. Maruyama, H. Watanabe, S. Shuto, G.J. Hemink, R. Shirota, S. Watanabe and F. Masuoka, "A 0.67 μm^2 Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell) For 3V - only 256Mbit Nand EEPROMs", (IEDM Tech. Dig. Dec. 11-14, 1994, PP. 61-64), pp. 3.6.1 - 3.6.4.					
RB	BR	William D. Brown, Joe E. Brewer, "Nonvolatile Semiconductor Memory Technology" "A Comprehensive Guide to Understanding and Using NVSM Devices", (IEEE Press series on microelectronic systems 1998), pp. 21-23.					
RB	BS	Rebecca Mih et al., "0.18 μm Modular Triple Self-Aligned Embedded Split-Gate Flash Memory", 2000 Symposium on VLSI Technology, Digest of Technical Papers.					
RB	BT	K. Naruke, S. Yamada, E. Obi, S. Taguchi, and M. Wada, "A New Flash-Erase EEPROM Cell With A Sidewall Select-Gate On Its Source Side", (IEDM Tech. Dig. Dec. 3-6, 1989, PP. 603-606), pp. 25.7.1-25.7.4.					
Examiner		Date Considered 06/25/04					
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